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MULTI-BAND INFRARED CAMERA SYSTEMS

David Sarnoff Research Center

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The program resulted in one of the first IR camera systems to utilize a unique MOS addressable focal plane array with full TV resolution, electronic control capability, and windowing capability. Two systems were delivered, each with two different camera heads: a Stirling-cooled 3-5 um band head and a liquid nitrogen-cooled, filter-wheel-based, 1.5-5 um band head. Signal processing features include averaging up to 16 frames, flexible compensation modes, gain and offset control, and real-time dither. The primary digital interface is a Hewlett-Packard standard GPID (IEEE-488) port that is used to upload and download data. The FPA employs an X-Y addressed PtSi photodiode array, CMOS horizontal and vertical scan registers, horizontal signal line (HSL) buffers followed by a high-gain pre-amplifier and a depletion NMOS output amplifier. The 640 x 480 MOS X-Y addressed FPA has a high degree of flexibility in operational modes. By changing the digital data pattern applied to the vertical scan register, the FPA can be operated in either an interlaced or non-interlaced format. The thermal sensitivity performance of the second system's Stirling-cooled head was the best of the systems produced.

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Section I

INTRODUCTION

This report summarizes a multi-year research and development program at the David Sarnoff Research Center sponsored by the Air Force Rome Laboratory, Hanscom Air Force Base.

The program resulted in one of the first IR camera system utilizing a unique MOS addressable focal plane array with full TV resolution, electronic exposure control capability, and windowing capability. Two systems were delivered. Each with two different camera heads: a Stirling-cooled 3-5 μm band head and a liquid nitrogen-cooled, filter-wheel-based, 1.5-5 μm band head.

Signal processing features include averaging up to 16 frames, flexible compensation modes, gain and offset control, and real-time dither. The primary digital interface is a Hewlett-Packard standard GPIB (IEEE-488) port that is used to upload and download data. The laptop computer controls the camera head via an RS-232 interface and the video processor via a VME bus interface. The internal VME backplane features 20 double-width ports, 9 of which are free for future upgrades.

The FPA employs an X-Y addressed PtSi photodiode array, CMOS horizontal and vertical scan registers, horizontal signal line (HSL) buffers followed by a high-gain pre-amplifier and a depletion NMOS output amplifier. All external connections on the FPA are static protected using the standard CMOS practice of providing separate on-chip reverse-biased diodes.

The 640 x 480 MOS X-Y addressed FPA has a high degree of flexibility in operational modes. By changing the digital data pattern applied to the vertical scan register, the FPA can be operated in either an interlaced or non-interlaced format. The integration time can be varied over a wide range (from ~60 μs to > 30 ms) by shifting a double pulse train through the vertical scan register. In these camera systems, the imager is operated in the non-interlaced mode.

The thermal sensitivity performance of the second system's Stirling-cooled head was the best of the systems produced. This system had an NEΔT = 0.13 C with the 3- to 5-μm filter and an f/1.8 cold shield (no lens).

The authors would like to acknowledge the contributions of several individuals whose designs contributed to the successful completion of this program: Rob Bassman, Peter Coyle, Ben Esposito, Howard Feder, Harvey Gilmartain, Joe Groppe, Gary Hughes, Peter Levine, Tim Pletcher, Don Sauer, Frank Shallcross, Paul Smalser, and Tom Villani.

Section II

THE ADI PASSIVE INFRARED CAMERA SYSTEM

A. SUMMARY

The ADI Passive Infrared Camera Systems marry full TV resolution PtSi focal plane technology to powerful digital signal processing electronics and high-performance optics. The system has the flexibility to accommodate valuable future upgrades and spin-offs.

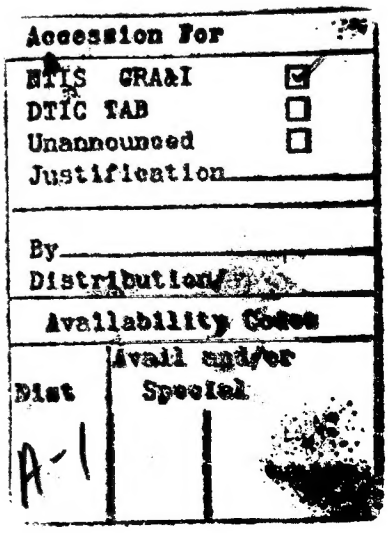
B. FOCAL PLANE ARRAY

The focal plane array (FPA) offers wide dynamic range, high resolution, and a high degree of spatial uniformity. Our MOS-multiplexed array offers greater operational flexibility than CCD multiplexers. The focal plane features a novel multiplexer design with very wide dynamic range and excellent MTF characteristics inherent to MOS multiplexers.

The MOS architecture is highly flexible, and provides for several useful spin-offs in the future. Most desirable of these spin-offs is future LWIR operation using Iridium or Germanium silicide detectors cooled to 40-50°K. (In fact, the array can operate all the way down to 4.2°K without degradation of MTF.) The availability of programmable readout modes is another degree of flexibility. Capability for electronically variable integration time, continuous electronic pan and zoom, and high frame rate operation are incorporated in the focal plane design.

C. CAMERA HEAD

The camera head electronics provide generation of all focal plane clock signals, video signal processing (including correlated double sampling) up to and including 12-bit A/D conversion, and all-digital outputs. The noise contributions and drift from the electronics are small compared to the stringent overall system noise requirements. Stable timing elements and precision low-noise amplifiers and associated passive components are used in the system. Correlated double sampling and a final line clamp eliminate 1/f noise.



D. SIGNAL PROCESSING

The signal processor has features that greatly enhance signal processing currently applied to PtSi cameras. Key features that optimize detection of weak signals include increased nonuniformity compensation (over the usual 16-frame-sum single-point correction), and sliding frame-averaging capability. The processor provides all required functions using cost-effective OEM video processing modules. The control system is expandable for future upgrades. The system offers the additional advantage that many compatible OEM boards are already available for future upgrades.

E. IR OPTICS

The wide band (1.5- to 5.5-μm), 200-mm, f/1.85 lens with 100% cold stop efficiency is an unusual design. The lens uses over-sized optics to provide the necessary cold stop efficiency and six elements for achromatization over the wide spectral bandwidth and f/# of 1.85.

The Stirling Head is supplied with a 3.0 to 5.0 μm filter installed. The Multiband Head is supplied with eight selectable filters.

F. DEWAR SYSTEM

Each system includes a wide spectral-band (3-5 μm) Stirling-cooled sealed camera capable of 65 to 80° K operation, and a liquid nitrogen-cooled research dewar with an eight-position filter wheel. The metal-sealed dewar design incorporates our proprietary getter configuration that has a five-year hold time. The research dewar includes user-replaceable filters and a filter wheel mechanism that features precise sub-pixel filter location repeatability (since slight spatial variations on the filter surfaces affect uniformity correction coefficients).

G. POST-DELIVERY SUPPORT, SCHEMATIC DIAGRAMS

The equipment is designed to be serviceable at the customer's premises. Operating instructions, schematic diagrams, and timing diagrams were delivered with each camera.

Section III

TECHNICAL APPROACH

A. CONFIGURATION AND SYSTEM INTEGRATION

Each system comprises five major components: a sealed camera assembly with associated electronics, a multiband liquid nitrogen-cooled dewar assembly with associated electronics, a lens assembly, a video processor/controller/power supply unit and a laptop computer for controlling the system (See Fig. III-1).

The user assembles a complete camera system by connecting either the Stirling-cooled camera assembly or the multiband, LN_2-cooled dewar camera assembly to the video processor/controller/power supply unit with three cables. The main mechanical structure of the head (mounting points, etc.) is a housing that normally remains attached to the sealed cooler or multiband dewar. The housings are different for the two types, in order to accommodate different cooler dimensions, but the mounting points are compatible.

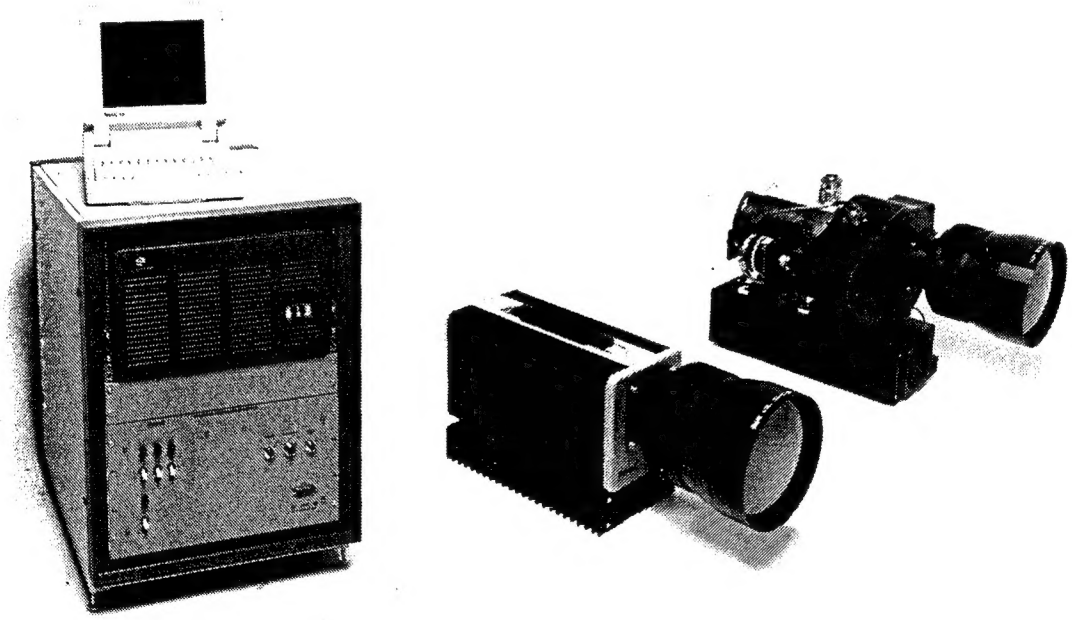


Figure III-1. *Overall system configuration.*

The video processor is based on a set of video processing boards (manufactured by Datacube, Inc., Peabody, MA) with an internal VME bus microcomputer card. All computations are done to at least 16-bit accuracy. The primary digital interface is a Hewlett-Packard standard GPIB (IEEE-488) port that is used to upload and download data. The laptop computer controls the

camera head via an RS-232 interface and the video processor via a VME bus interface. The internal VME backplane features 20 double-width ports, 9 of which are free for future upgrades.

All of the software necessary for digital processing and communication through the GPIB port is supplied.

Three cables connect the processor/controller/power supply unit to the head: one for power and control, one for digital video output and the other for Stirling cooler power or filter wheel control, depending on the camera head used.

B. 640 x 480 FOCAL PLANE ARRAY

1. 640 x 480 FPA Design

A functional architecture diagram of the 640 x 480 FPA is shown in Fig. III-2. The FPA employs an NMOS X-Y addressed PtSi photodiode array, CMOS horizontal and vertical scan registers, horizontal signal line (HSL) buffers followed by a high-gain pre-amplifier and a depletion NMOS output amplifier. The design is based on a 1.5-μm single-poly double-level-metal N-well CMOS process, as described in Section III-B.4. The output of the source follower is connected to one of eight vertical signal lines in order to reduce the capacitive load on the source follower to 15 pF. This maintains good transient response so that correlated double sampling can be performed later in the video amplifier. A signal MUX register is used to connect one of the eight vertical signal lines to the output amplifier via one of the transmission devices QM1-QM8 that have an "on" resistance of 30 Ω. The on-chip source-follower load has an impedance of 2000 Ω. The signal multiplexer feeds into an amplifier that provides a voltage gain of 5 and a low-impedance output.

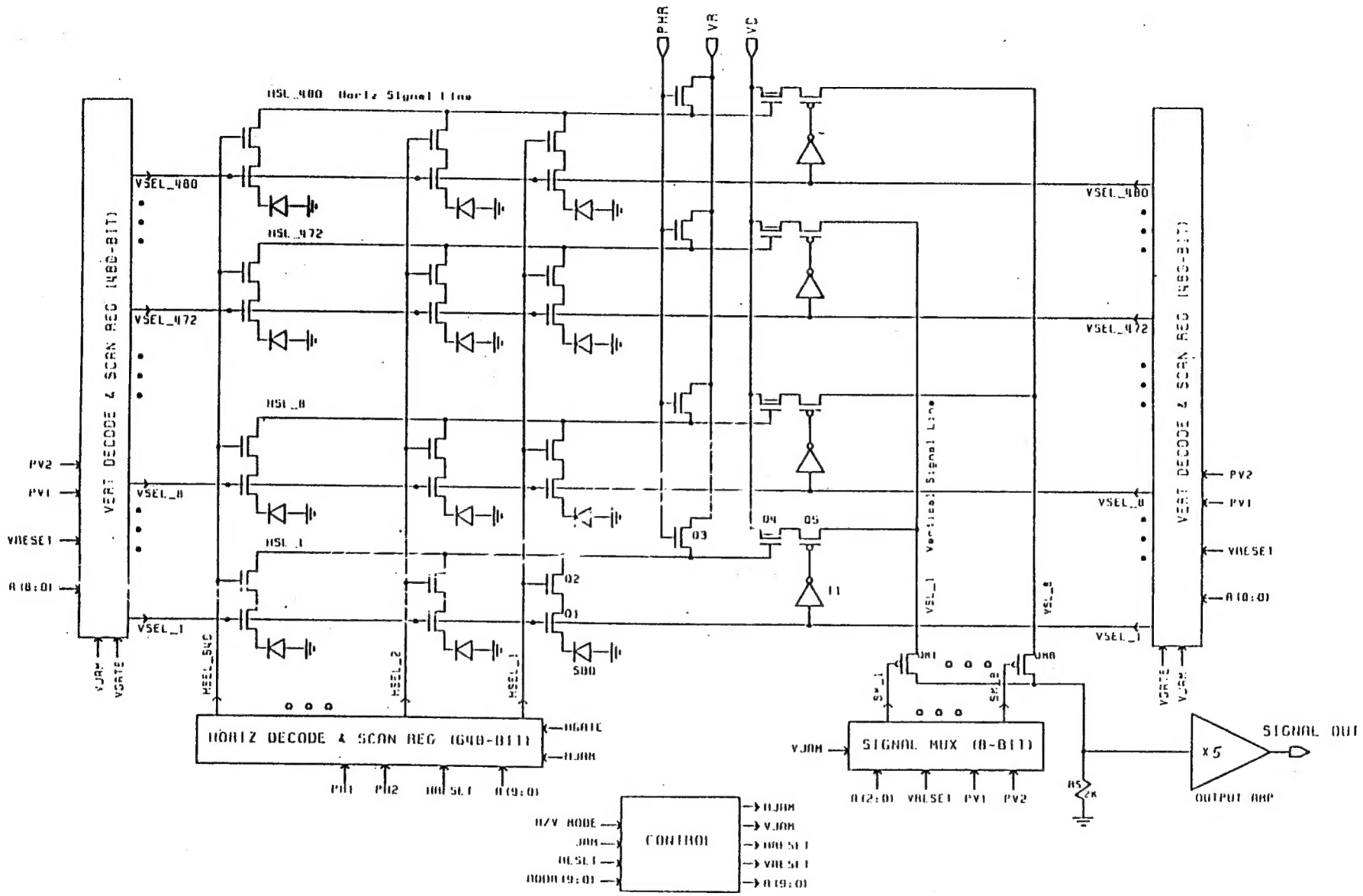


Figure III-2. *640 x 480 focal plane array functional architecture.*

a. Horizontal and Vertical Scan Registers

A 640-bit CMOS horizontal scan register detailed in Fig. III-3 is used to address one of the horizontal select lines (HSEL_1 - HSEL_640). It is clocked at the horizontal readout rate by two non-overlapping clock phases PH1 and PH2, which are generated on-chip from a single TTL level input horizontal clock. (See Fig. III-4) The initial state of this register is controlled by an external 10-bit address bus, which is decoded on-chip together with RESET and JAM control signals. Details of this operation are described below.

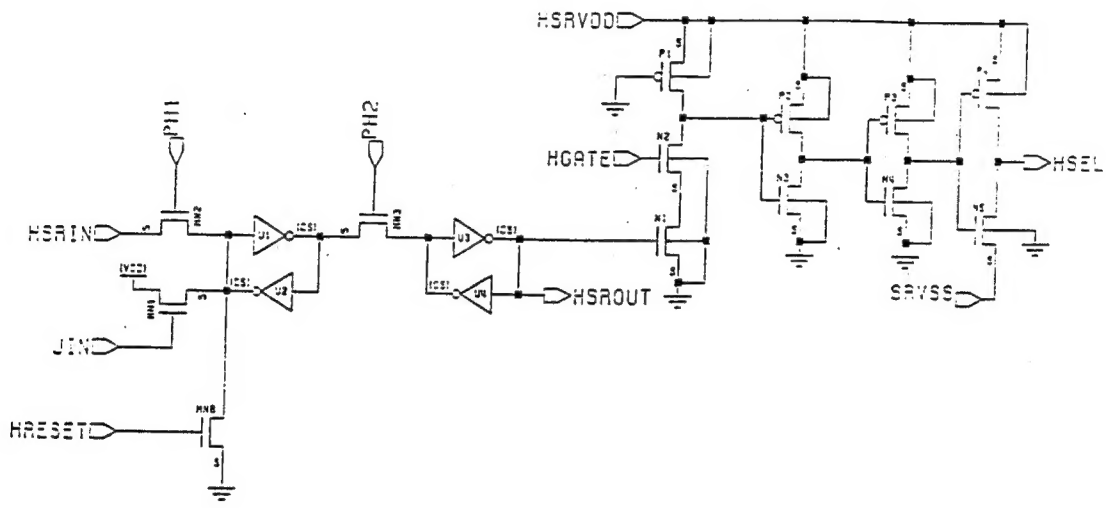


Figure III-3. *Horizontal scan register schematic.*

The 480-bit CMOS vertical scan registers, shown in Fig. III-2, are used to select a line of pixels by turning on one of the vertical select lines (VSEL_1 - VSEL_480). They are clocked by two non-overlapping asymmetrical vertical clock phases PV1 and PV2, which are timed to switch during the horizontal blanking period. The vertical select line also controls a PMOS switch (e.g., Q5 through inverter I1) that connects the depletion NMOS source follower (Q4) to a vertical signal line (VSL_1). The polysilicon vertical select lines are driven from both ends of the FPA to reduce the time constant.

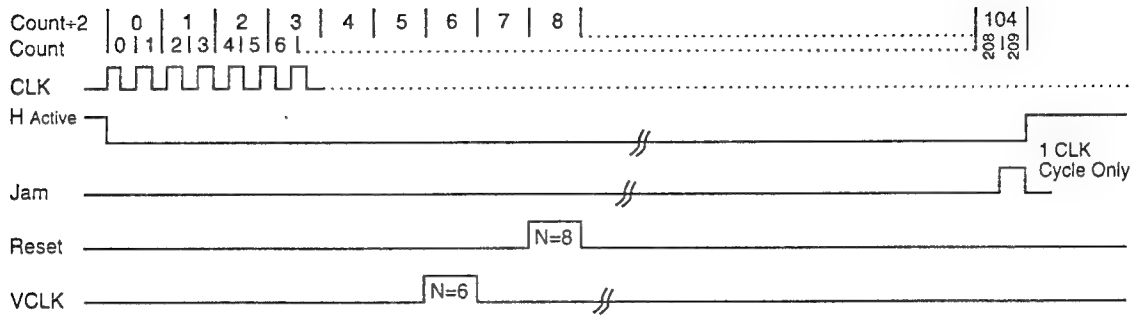


Figure III-4. *Horizontal rate timing diagram.*

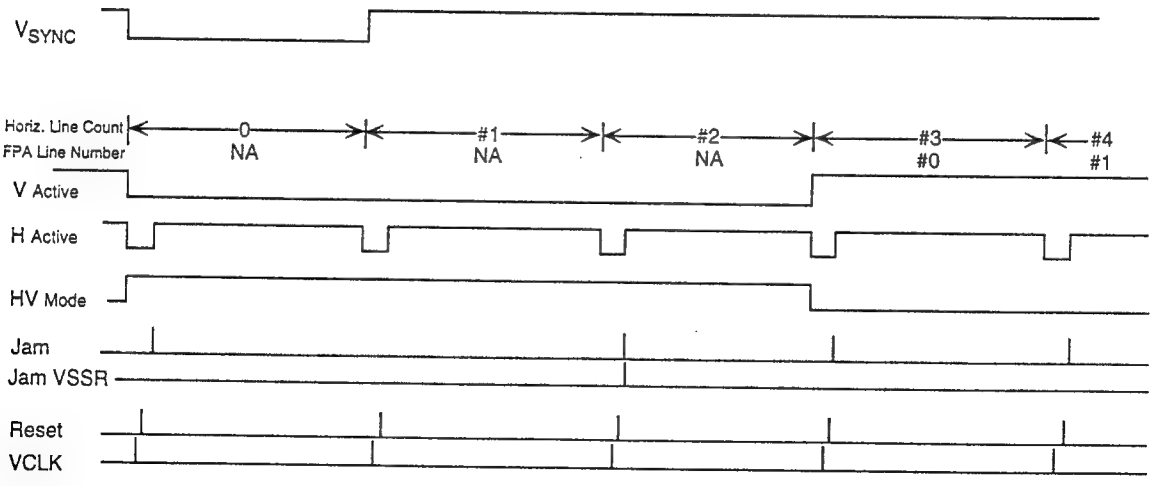


Figure III-5. *Vertical rate timing diagram.*

A source follower configuration is used rather than an inverter or cascode amplifying configuration for the HSL buffer for two reasons. First, the source follower provides the lowest input capacitance on the signal line due to the effect of positive feedback through C_{gs}. Second, the source follower provides much better gain uniformity than an inverting configuration since it is less sensitive to g_m variations. With an inverting configuration, the voltage gain A_v is directly proportional to g_m and therefore the gain sensitivity $(DA_v/A_v)/(Dg_m/g_m) = 1$. For the source follower, the gain sensitivity in this case is $1/(1 + g_mR_L)$. Since g_mR_L is typically > 10, the gain sensitivity of the source follower to g_m variations is an order of magnitude less than the inverting amplifier configuration. The source follower device size is a tradeoff between minimizing input gate capacitance and maximizing g_m in order to achieve good transient response and reduce thermal noise in the MOS channel.

Due to the relatively large size of the source follower devices, the g_m variations are < 2%. Therefore, the vertical line-to-line gain variations using this architecture are < 0.2% (on the same order of magnitude as existing detector-to-detector variations). These multiplicative variations are removed in the video processor.

b. FPA Control Logic Operation

The operating modes of the 640 x 480 FPA are controlled by the H/V MODE, JAM, RESET, and ADDR(9:0) inputs shown in Figs. III-2 and III-5. The H/V MODE control input places the device in either a horizontal or vertical mode. In the horizontal [vertical] mode, JAM controls HJAM [VJAM], RESET controls HRESET [VRESET], and the 10-bit address ADDR(9:0) applied to the chip may be latched into an internal horizontal [vertical] address register. During horizontal blanking, the horizontal scanning register is initialized by first resetting all bits to a "0" state with HRESET, and then applying HJAM to force a "1" state at the position currently stored in the horizontal address register. If a second horizontal address is latched into the chip, and the additional "1" jammed into the horizontal scanning register before it is clocked serially, a reduced integration time results.

The horizontal decoder is a binary decoder whose outputs are gated with HJAM to produce the JIN input shown in Fig. III-3. This figure is a detail schematic of one stage of the horizontal scanning register. The horizontal select lines HSEL are generated by ANDing HGATE with the scan-register output, which is followed by a CMOS driver that has controlled levels (HSRVDD and SRVSS) for the high and low HSEL potentials. Figure III-6 shows the timing relationships between the pulses appied to the FPA at the pixel rate.

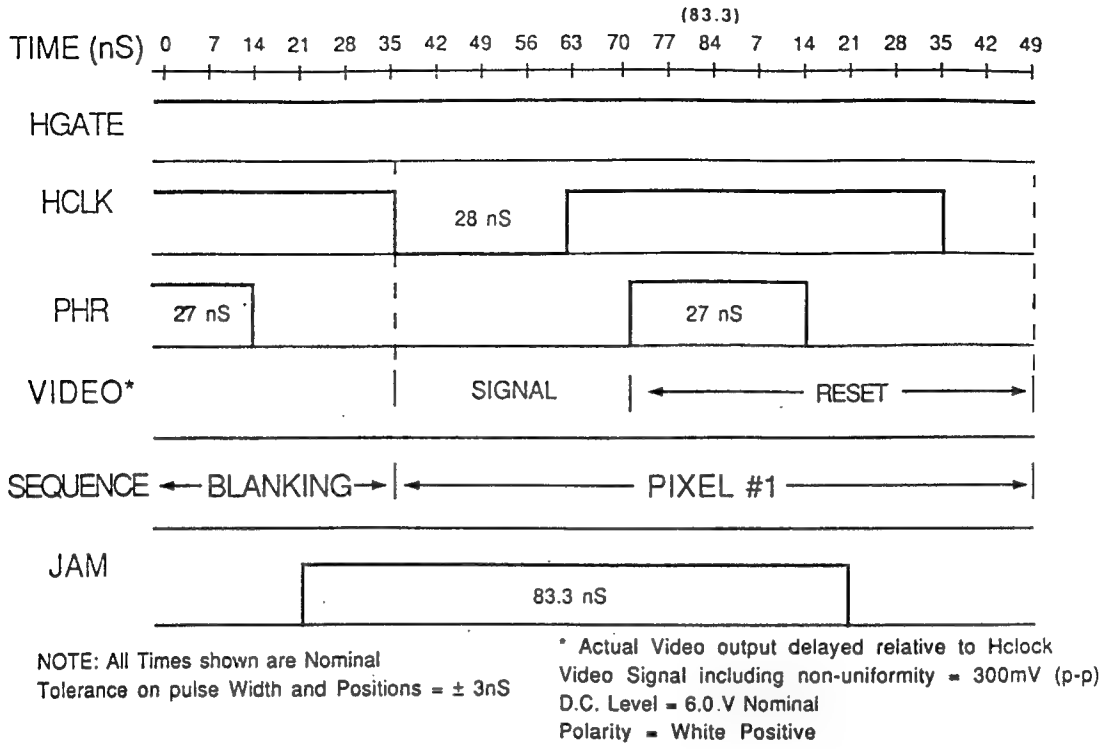


Figure III-6. *Pixel rate timing diagram.*

c. PtSi Cell Design

A composite layout of four 24-μm x 24-μm PtSi photodiode cells using an NMOS X-Y addressed readout and based on 1.5-μm layout design rules is shown in Fig. III-7. In each cell, the active PtSi area is 216 μm^2 yielding an optical fill factor of 216/576 = 38% as drawn.* An N^+ guard band surrounds the active PtSi Schottky barrier detector and merges with the source region of a vertical select transistor Q1. The vertical gate line connection for Q1 runs horizontally in polysilicon. A horizontal select transistor Q2 is in series with Q1. The gate of Q2 is connected by means of a polysilicon contact and metal via to the horizontal gate line, which runs vertically using metal 2. The drain of Q2 is connected to the HSL, which is metal 1 and is located on top of the polysilicon vertical gate line. A first-layer metal reflector (not shown) is defined to cover the PtSi active detector area. Based on this layout, the various components comprising the total capacitance on the HSL have been calculated for one cell:

*A fill-factor of 50% has recently been realized with this cell design by applying tighter design rules (for example, rules which yield 1.2 μm metal lines).

1.	N^+ to P^- substrate depletion capacitance	Area	0.87 fF
	(Vpn = -5V) Periphery (Sidewall)		1.80 fF
2.	C_{gd} overlap for Q2 drain		0.50 fF
3.	Metal 1 to Poly (or active area)	Area	1.74 fF
	Periphery (Fringing)		2.41 fF
4.	Metal 2 to Metal 1	Area	0.10 fF
	Periphery (Fringing)		0.67 fF
5.	Metal 1 to Field	Area	0.36 fF
	Periphery (Fringing)		0.50 fF
	Total signal line capacitance per cell:		8.90 fF
	(Note: 1 fF = 10^{-15} Farad)		

Based on this calculation for a single cell, the total HSL capacitance including the loading effect of the source follower line buffer is:

$$C_{HSL} = 640 \times 8.9 \text{ fF} + 0.35 \text{ pF} = 6.1 \text{ pF}$$

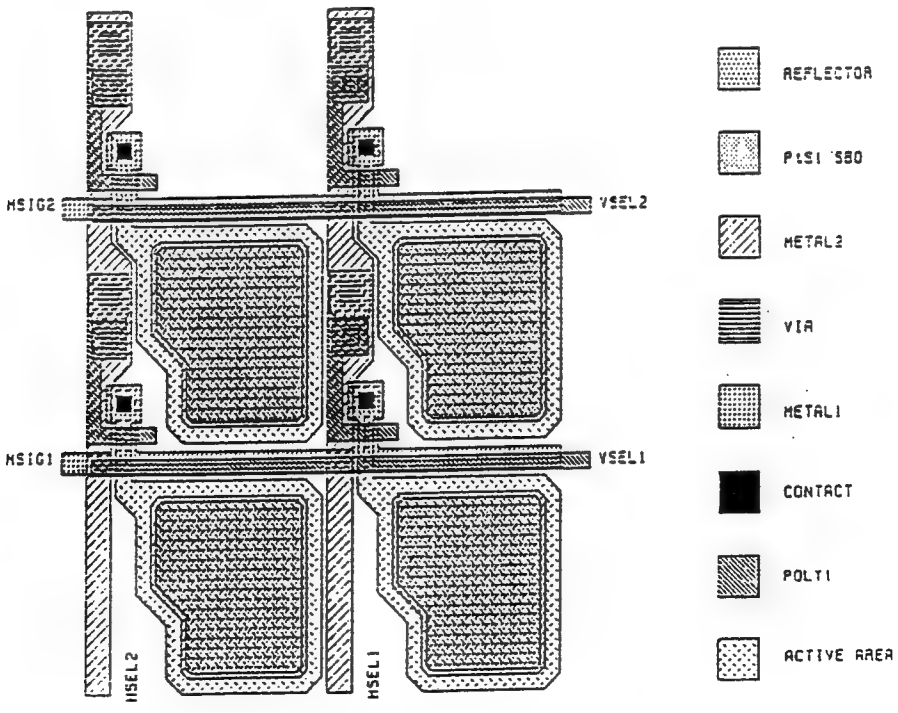


Figure III-7. *Layout of a 2 x 2 matrix of cells.*

d. Non-Linear Response

The detector/multiplexer design structure features a "soft" logarithmic saturation characteristic that provides nonlinear response over an ultra-wide dynamic range. When the integrated photocharge exceeds 1.2×10^6 electrons, the source of vertical select transistor Q1 falls below 0.2 V, which leads to substantial subthreshold leakage current in Q1 proportional to exp(-qV/kT). Conversely, the photodiode voltage V increases logarithmically by approximately 20 mV (q ln(10) / kT) per decade. (In this nonlinear regime, the photodiode reaches a steady-state voltage V determined by equality of the photocurrent and leakage current.) This principle of operation has been applied extensively in ultra-wide dynamic range visible arrays. This nonlinear FPA response is combined with compression of the excess linear dynamics range (see Section III- E-3c) to produce at least 50:1 compression of the overall camera response to signals above the 2000:1 linear dynamics range.

e. Static Protection

All external connections on the FPA are static protected using the standard CMOS practice of providing separate on-chip reverse-biased diodes connected between the bonding pads and the substrate and positive rails for positive and negative polarity protection. The FPAs should be handled with the same precautions as CMOS logic devices.

2. 640 x 480 FPA Performance

Table III-1 summarizes the performance specifications for our 640 x 480 MOS X-Y addressed IR FPA.

Table III-1. *Specifications for 640 x 480 FPA*

PtSi Detector Parameters	
Emission Factor	$C_1 > 0.2$
Cut-off Wavelength	$\lambda c > 5.2$ μm
Breakdown Voltage	$Vb > 15$ V
RMS Responsivity Non-uniformity	~ 0.5%
FPA Array Specifications	
Array Size	640 x 480 pixels
Effective Pixel Spacing	24 μm x 24 μm
Optical Fill Factor	38% (24- x 24-μm pixel size)*
Die Size	17.3 x 13.9 mm (682 x 548 mils)
P_d @ fc = 12 MHz (multiplexers)	15 mW
Integration Time	Electronically variable from line period (60 μs) to >30 ms
Operating Temperature	4.2°K to 80°K
Output Multiplexer Parameters	
Electron Sensitivity	0.1 mV/electron
Linear Dynamic Range	82 dB
P_d @ 12 MHz (output amplifier)	95 mW (typ)
Maximum Horizontal Clock Rate	>12 MHz
Output Impedance	200 Ω (typ)

3. Operational Modes

The 640 x 480 MOS X-Y addressed FPA has a high degree of flexibility in operational modes. By changing the digital data pattern applied to the vertical scan register, the FPA can be operated in either an interlaced or non-interlaced format. The integration time can be varied over a wide range (from ~60 μs to > 30 ms) by shifting a double pulse train through the vertical scan register. In these camera systems, the imager is operated in the non-interlaced mode. The full capabilities of the FPA's operating modes are described below for future system enhancements.

a. Non-Interlaced Format

The simplest operational mode for the FPA is accomplished by shifting a single pulse down the vertical scan register and clocking this register once during each horizontal blanking period. This causes each horizontal row of pixels to be read out in sequence, and the video image is

*Extendable to 50% with 1.2 μm design rules.

displayed non-interlaced with 480 lines/frame. This is the operational mode implemented in the delivered cameras.

b. Vertical Interlace Format

A standard 2:1 vertical interlace mode of operation may be accomplished by shifting a single pulse down the vertical scan register and clocking this register twice during each horizontal blanking period. This causes the readout of alternate horizontal rows in the array so that even and odd fields, each containing 240 lines, may be displayed in sequence.

c. Electronic IRIS (Variable Integration Time)

Because our 640 x 480 FPA design contains eight separate vertical signal lines, which may be independently selected by the signal MUX register, it is possible to vary the effective integration time by shifting a double pulse down the vertical scan register and timing the signal MUX register data so that only the HSL selected by the second pulse in the vertical scan register is connected to the output amplifier. In this mode of operation the first pulse shifted down the vertical scan register selects and resets a horizontal row of pixels before the same row is read out by the second pulse. Therefore, the integration time period for the pixels is determined by the time interval between the two pulses. The only restriction in this mode of operation is that the selected pulse spacing (integration time) cannot be a multiple of eight times the horizontal line period since this would cause two horizontal lines to be connected to the same vertical signal line simultaneously.

d. Electronic Pan

The focal plane provides electronic pan capability that can be used to support a dither operation. In this mode, each frame consists of the pixels inside a rectangular "window" within the 640 x 480 format. The location of the "1" forced into the horizontal shift register at the beginning of each line defines the left edge of the window (Section III-B-1b). The horizontal size of the window is equal the number of clock pulses per line applied to the horizontal shift register. Similarly, the location of the "1" forced into the vertical shift register defines the top edge of the window, and the number of vertical clock pulses per field determines the vertical size. For dither operation, the window is the central quarter of the imager.

A significant advantage of the MOS architecture is that, unlike the CCD architecture, detectors outside the window need not be read out.

4. Fabrication of FPAs

a. CMOS Processing

The FPAs used in this program are based on existing high-performance CMOS technology. The design employs N-well CMOS technology with one level of polysilicon and two levels of metallization, with 1.5-μm design rules (corresponding to the minimum allowable contact opening size). The wafer fabrication was done in the Sarnoff Integrated Circuit Facility, using the Optimetrix 8605H 5:1 stepper for the photolithography.

The basic CMOS process consists of N-well formation, active area definition and selective field oxidation, channel oxidation and polysilicon definition, P^+ and N^+ implantations, and contact and first-level metal definition. In the double metal process these steps are followed by interlevel dielectric deposition and planarization, via opening, second level metal definition and protect-layer deposition.

b. Schottky-Barrier Detector Processing

After contact definition and glass flow, the detector regions are etched to silicon, and the platinum layer is deposited onto the exposed silicon. The platinum films are annealed to form a layer of PtSi (about 20-Å thick) in the detector regions. The unreacted platinum outside the detector regions is then stripped.

The PtSi SBD structure is completed by depositing a suitable dielectric, such as SiO_2, and then depositing and defining the first-level metallization layer that includes the reflectors. The process is then finished with the interlevel dielectric deposition, via opening, second level metallization, and scratch-protect layer. The completed detector structure is illustrated in Fig. III-8. The final lithographic step is to open the bonding pad regions.

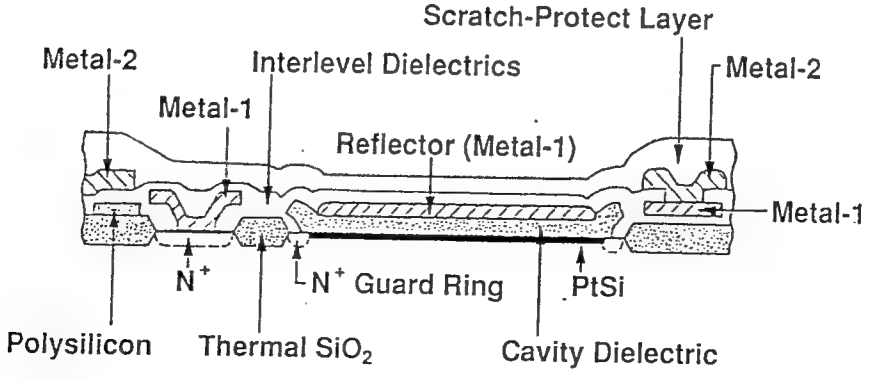


Figure III-8. *Cross-section showing detector structure.*

C. CRYOGENIC DEWARS

Two different types of camera dewar assemblies are provided: (1) A multiband dewar consisting of a liquid nitrogen cooled cold finger, a baffled cold shield assembly, and a remotely controlled cooled eight-position filter wheel; and (2) a sealed camera assembly with a closed-cycle Stirling cryogenic refrigerator, a baffled cold shield with a replaceable IR filter, and an all metal permanent vacuum dewar design.

1. Sealed Camera Assembly

The dewar Stirling cooler assembly is the Magnavox Model# MX7049 split-Stirling 2-W linear drive cooler, cold shield, cold filter, and temperature sensors. A drawing of the assembly is shown in Fig. III-9.

The cold-shield is a lightweight aluminum computer-designed structure of appropriate size to match the 200-mm lens and minimize cool-down time. A 3- to 5-μm IR bandpass filter is clamped in place by the cold-shield assembly and cooled by heat flow into the cold shield base. An AR-coated sapphire window is brazed to a kovar ring and welded to a stainless steel vacuum shroud that is bolted to the dewar body utilizing Helico-flex metal o-ring seals. The evacuation tube is sealed by a miniature all-metal vacuum valve that permits re-evacuation in the event of disassembly of the dewar (e.g., to install a different optical filter).

Our proven all-metallic seal vacuum dewar design eliminates rubber "o"-ring outgassing and deterioration problems. The vacuum integrity is ensured by using a non-evaporable electrically fired getter, mounted on the inside wall of the dewar cap. Once fired, this getter is activated and continues to absorb gasses even at room temperature. Our experience has shown that the getter overcomes the pressure rise due to residual outgassing of components and virtual leaks.

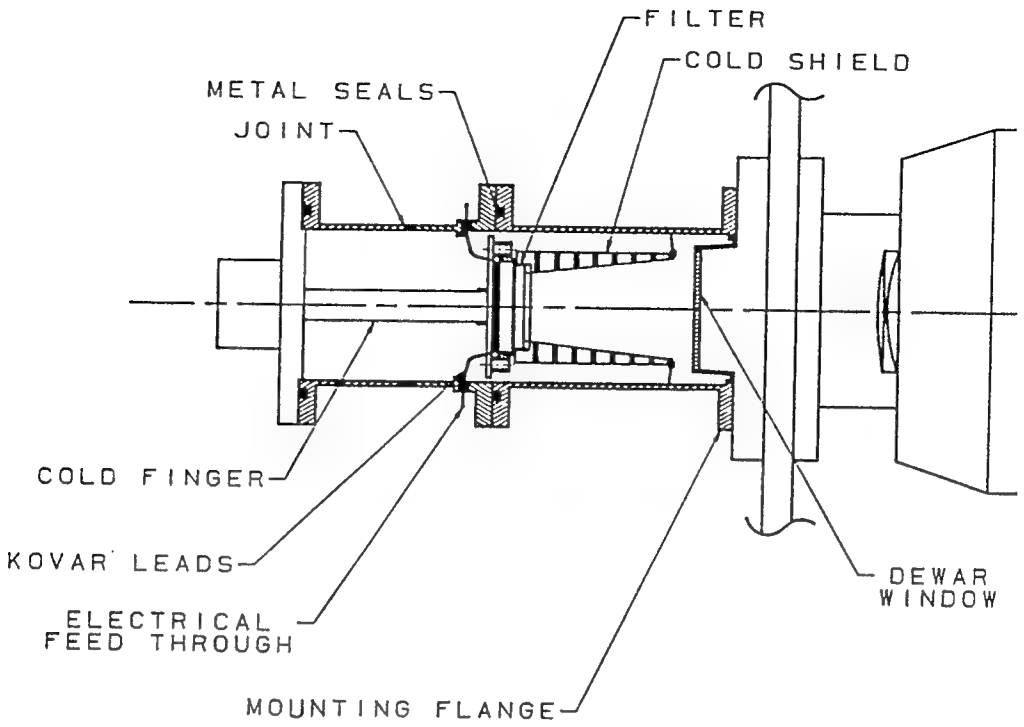


Figure III-9. *Layout of dewar cooler assembly.*

Electrical connections to the FPA and temperature sensors are provided by a set of ceramic feedthroughs welded into the dewar wall. Five-mil.-diameter, Teflon-coated, low-thermal conductivity constant wires are used to minimize heat flow to the cold head. A diode sensor and a resistive thermal device (RTD), which is a thin-film platinum resistive thermometer are used to monitor and control the cold finger temperature. The diode sensor is connected to a proportional-type motor speed control to regulate the cryogenic cooler's capacity, holding the cold finger at a constant temperature.

A custom-designed 40-pin lightweight gold ceramic package is used to mount the 640 x 480 element FPA to the cold finger with a wave-washer type spring force applied from the cold shield base (See Fig. III-10). Thermal contact is ensured by a 5-mil-thick indium gasket placed at the interface.

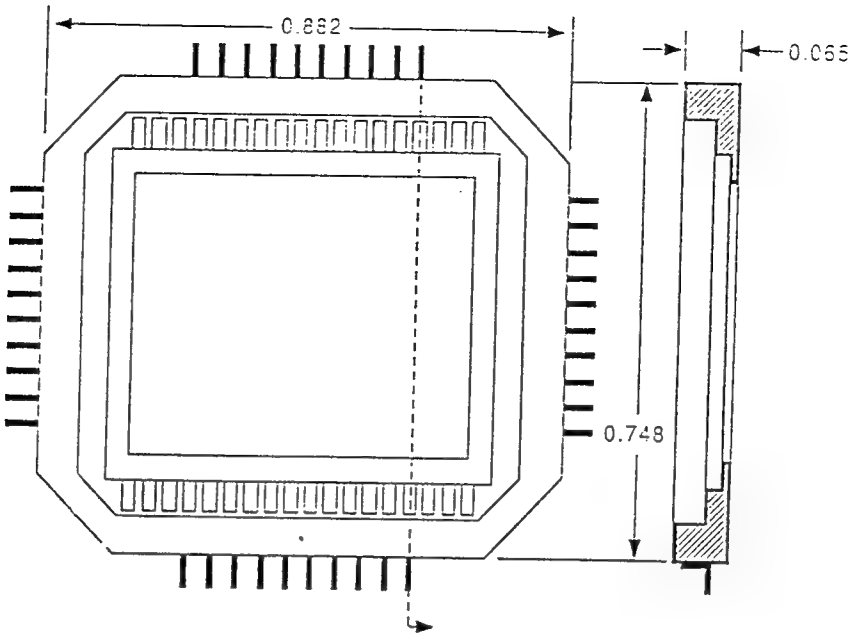


Figure III-10. *40-pin ceramic package for FPA.*

2. Multiband Camera Assembly

The multiband dewar utilizes a side-looking liquid nitrogen cooled cold finger with a 1.5-liter reservoir for at least 10-h hold time (See Figs. III-11 and III-12). The vacuum shroud is an "o"-ring-sealed type with a standard vacuum valve for re-pumpability. The cold finger accommodates the FPA and cold shield base clamp assembly as well as a cooled 8-position filter wheel. The bandpass filters mounted in the wheel are cooled by radiation to the filter wheel enclosure and intercept the incoming ray bundle through an aperture in the baffle assembly through which the filter wheel passes.

The filter wheel is driven by a thin stainless steel belt to isolate the cold wheel from the warm drive gear. The stepper motor is mounted outside the dewar and coupled mechanically to the drive gear. The wheel position is determined by an optical encoder coupled to the filter wheel.

Electrical connections are provided by two 22-pin hermetic connectors located on the vacuum shroud wall utilizing "o"-ring seals and MS-type mating connectors.

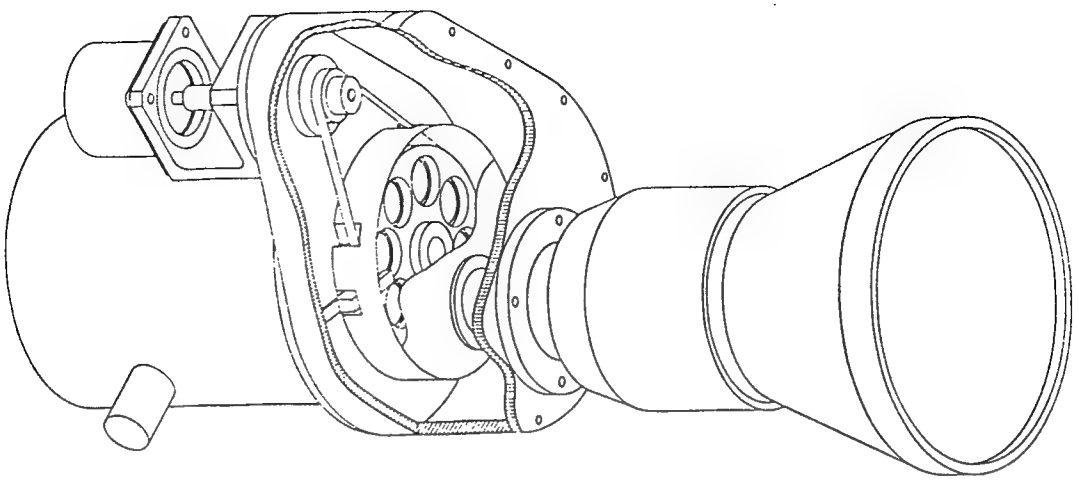


Figure III-11. *Multiband dewar isometric.*

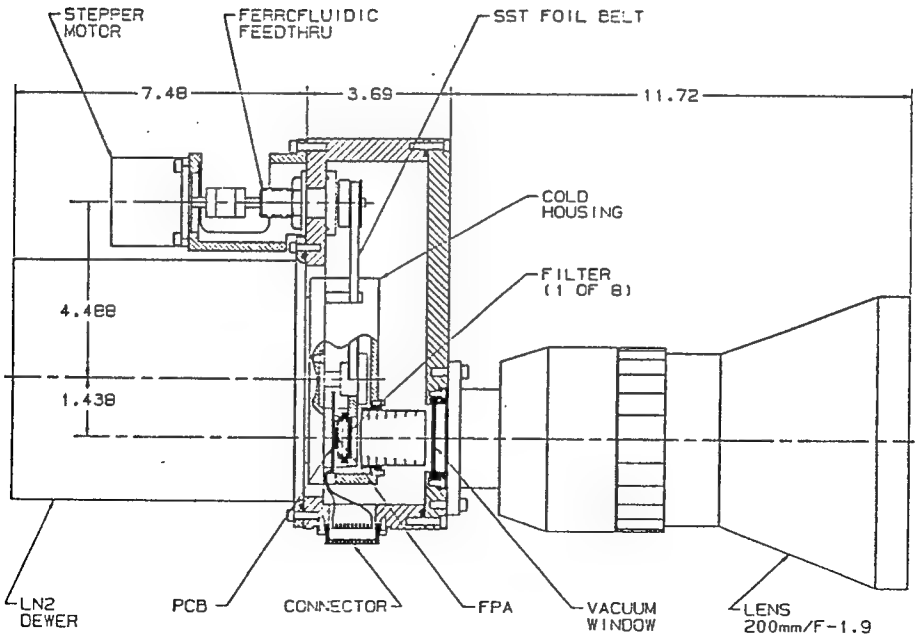


Figure III-12. *Cross-section of multiband dewar layout.*

D. IR LENS ASSEMBLY

The wide band (1.5 - 5.5 μm), 200-mm, f/1.85 lens with 100% cold stop efficiency without narcissus is an unusual design (See Fig. III-13). The lens has over-sized optics to provide the necessary cold stop efficiency and six elements for achromatization. In addition, an improved AR coating was used to achieve 70% transmission.

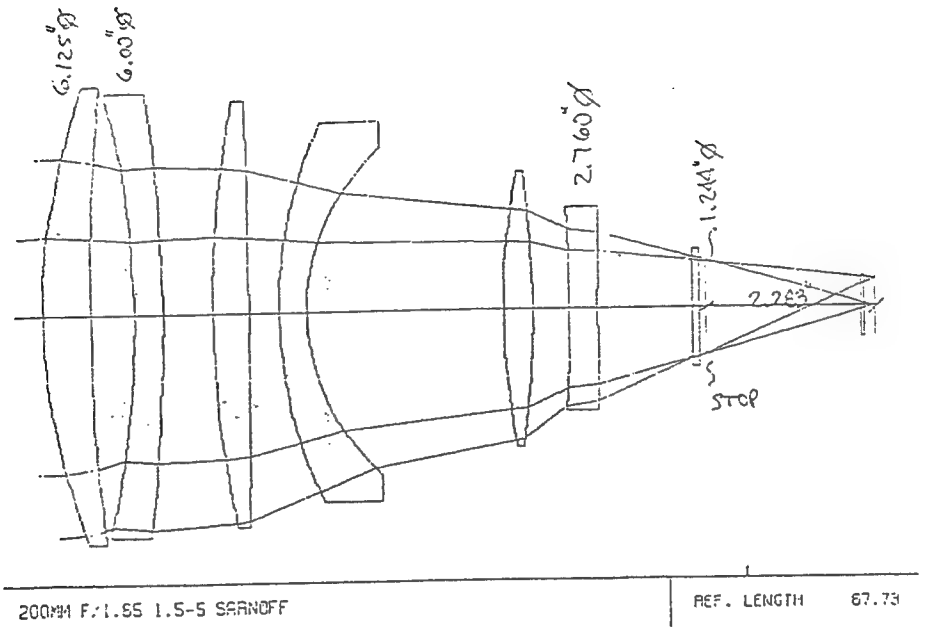


Figure III-13. *Layout of 200-mm f/1.85 lens.*

The complete optical system was optimized for minimal stray light with the aid of computer analysis. The program APART was applied by Breault Research to our initial optical design, and the final design of baffles and coatings was based on the results.

The mechanical interface to a camera or research dewar is a flange with externally accessible screws. Lens assemblies are fully interchangeable between camera heads.

The Multiband Camera Assembly has eight selectable filters as follows:

Filter No.	Bandpass
1	1.51 - 1.81 μm
2	1.80 - 2.00 μm
3	2.00 - 2.50 μm
4	2.61 - 2.84 μm
5	3.54 - 4.44 μm
6	4.21 - 4.30 μm
7	4.50 longpass
8	3.00 - 5.00 μm

E. CAMERA HEAD ELECTRONICS

Each camera head includes an electronics module that is an integral part of the camera head assembly.

1. Camera Head Interface

The camera head electronics operate the MOS imager, condition the analog output and convert it to 12-bit digital form, and provide master timing for the video processor/control unit.

Inputs to the head electronics from the processor/control unit consist of dc power and a data bus to program the operating mode of the camera head, including high/normal gain, linear/non-linear processing and optical filter selection.

Outputs consist of a 12-bit digitized data bus with horizontal and vertical sync pulses and clock signals for the processor control unit. A block diagram of the camera head electronics is shown in Fig. III-14.

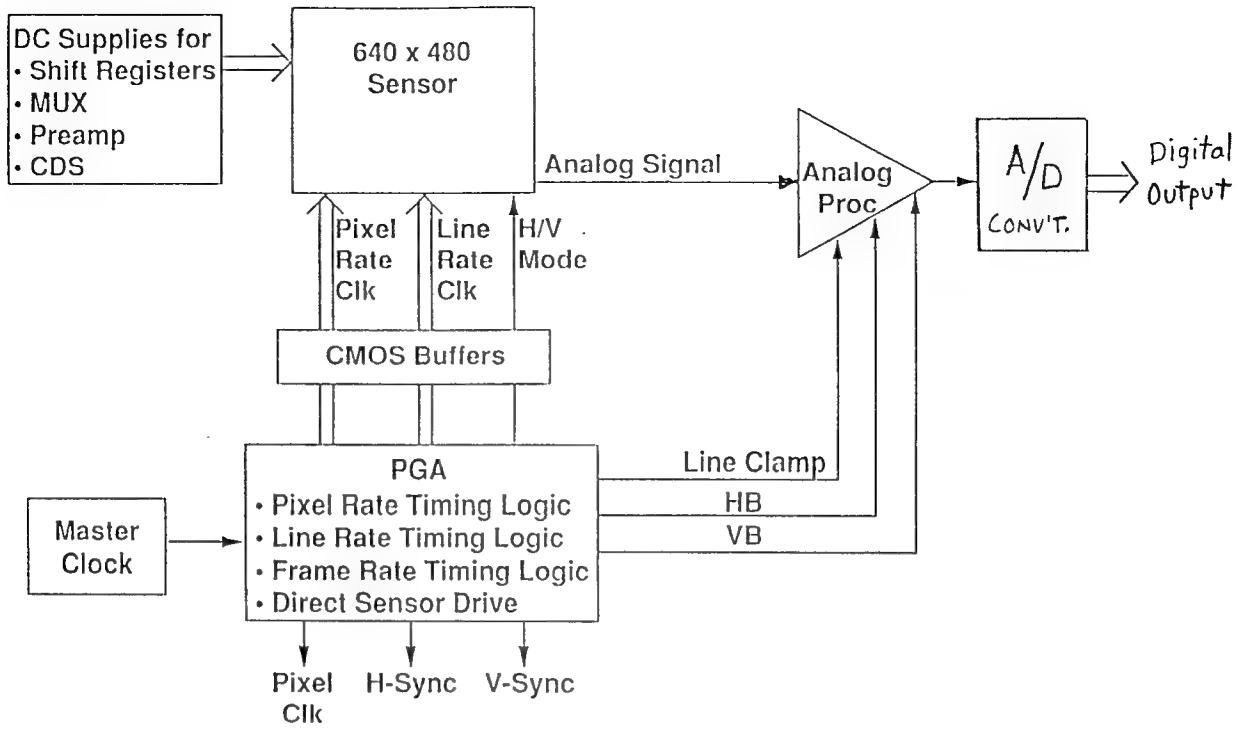


Figure III-14. *Block diagram of camera electronics.*

2. CMOS Imager Timing Circuits

a. Master Oscillator

Digital timing is derived from a crystal oscillator. All signals are derived from this master oscillator. Pixel rate clock circuits, such as the CDS timing section, incorporate a multi-tap digital delay line to derive finely timed phase-delayed edges from the master oscillator. There are no monostables or other R-C controlled timing elements in the camera head.

b. Scan Register Drive

The horizontal and vertical scan registers are the heart of the internal timing and control of the MOS imager. The clock signals to these registers govern the sequence of line and pixel selection. For a detailed description of the operation of these registers, refer to Section III-B.

The vertical register operates at 14475 Hz (483 x 29.97 Hz) with the scan commencing at line 1 for 30-Hz operation. (Three inactive lines are required by the digital processor.) The processor/control unit converts the scan mode to RS-170 standard 15734.3 Hz horizontal line rate with interlace for display purposes.

3. Video Signal Path

A block diagram of the complete video signal path in the camera head is shown in Fig. III-15. It is designed to provide low noise and low drift.

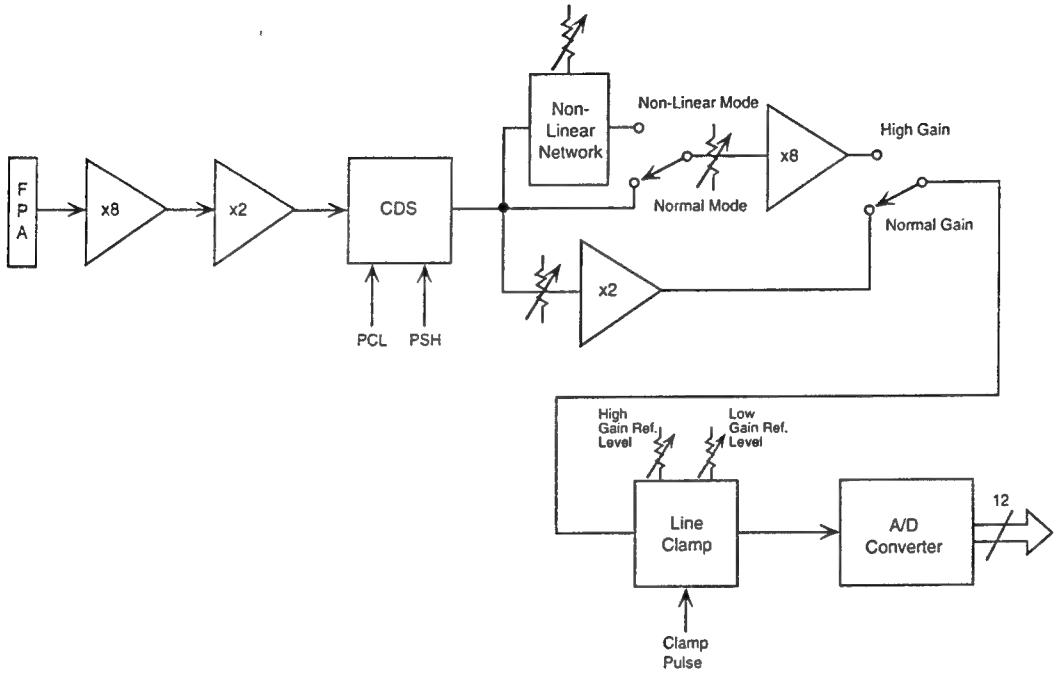


Figure III-15. *Block diagram of video signal path.*

There are three modes of operation: a normal linear mode, a high gain linear mode, and a high gain non-linear mode. Both the normal and high gain non-linear modes allow the full range of the FPA output to be digitized. In the high gain linear mode, only the lower quarter of the FPA output is within the range of the A/D converter.

a. Preamplifier

A precision preamplifier with a gain of 8 is mounted immediately outside each laboratory dewar and sealed cooler assembly. The preamplifier is a Comlinear CLC502, which features 150-MHz small-signal bandwidth, 2.0 $nV/Hz^{1/2}$ wideband noise, and the capability to drive a terminated 75-Ω cable.

b. Correlated Double Sampling

The signal from the preamplifier is received by an amplifier with a gain of 2. This amplifier also provides a low source impedance for the CDS circuit.

c. Video Amplifier

The video amplifier has a maximum gain of 2 or 8, depending on operating mode. Internal adjustments reduce the gain below these levels so that the full FPA output fits in the range of the A/D in the normal gain mode. The input to the high gain amplifier can be selected from either the linear or non-linear network. The break point of the non-linear network is set to compress the maximum output of the FPA to be within the range of the A/D converter.

d. Line Clamp

The line clamp is an ac-coupled unity gain buffer stage that removes dc offset drifts and sets the dc level of the video for proper A/D conversion. The clamp operates once per line during horizontal blanking, but its time constant is much longer so as not to convert high-frequency noise into low-frequency noise streaks. Different clamp reference sources are used for the high gain and normal gain modes.

e. Analog to Digital Conversion

The analog to digital converter is a Comlinear CLC 935 12-bit, 15-MHz, hybrid operating at 12.304 MHz in this system. The converter output is connected to differential TTL line drivers capable of driving 100 ft. of twisted pair cable.

4. Power Supplies

To ensure immunity from power supply, cable, and connector variations, the dc power inputs incorporate RFI filters, and in critical areas, are re-regulated to lower voltages. Separate supplies are used for analog and digital applications. The power inputs are +/-5 Vdc for the digital circuits, and +/-15 Vdc for the analog circuits.

F. PROCESSOR/CONTROL/POWER SUPPLY UNIT

The video image processor includes an assortment of image processing boards purchased from Datacube Corporation and two Sarnoff proprietary boards. The system features a graphical user interface (GUI) that allows users to interact with the system in an easy, intuitive fashion. The video image processor outputs a 640 x 480, interlaced image that can be displayed on any standard RS-170 video monitor. Figure III-16 is a block diagram of the camera- processor system.

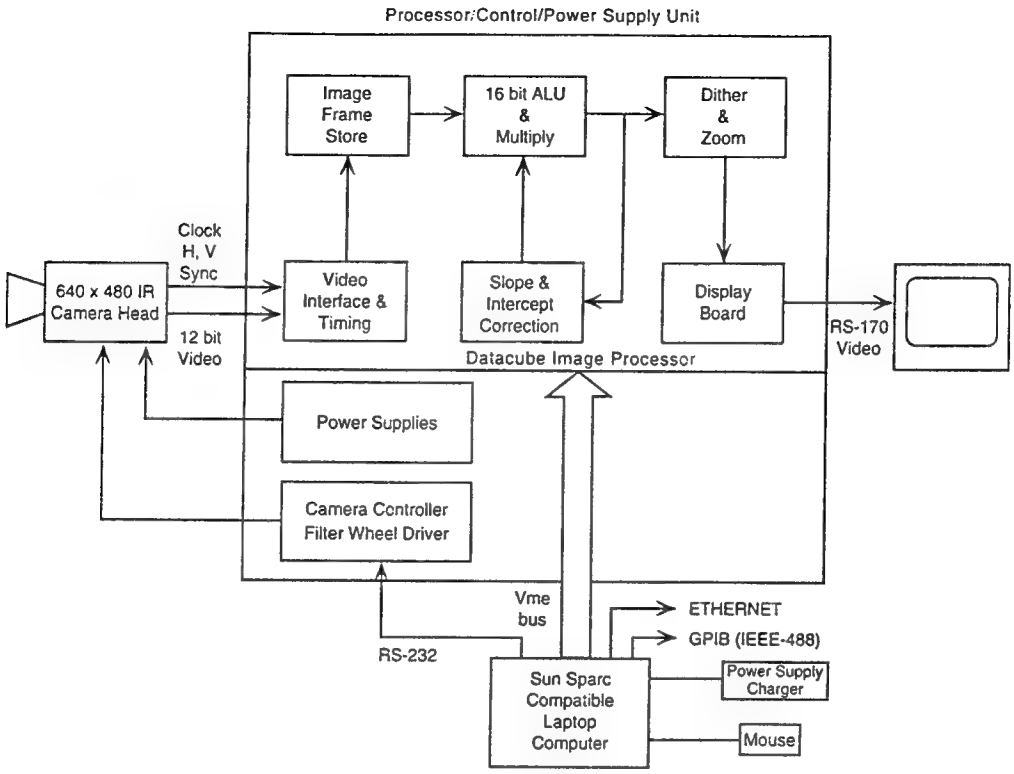


Figure III-16. *Block diagram of camera-processor system.*

The host computer is a Sun Sparc compatible laptop computer manufactured by RDI Computer Corporation. The computer features a 1100 x 900, LCD screen, a 240-Mbyte hard disk, a 1.44 floppy disk, and SunOS 4.1.1. The host computer operates in either Sunview or Sun Windows.

The controller contains the camera power supplies and means to select camera operating modes and any of the eight optical filters available in the multiband head. The host reads and writes bytes to the controller using an RS-232 port to instruct the controller to change operating modes and filters in the camera head.

The host provides a GPIB port that can connect to a GPIB bus as a slave device. Any remote computer, capable of acting as a GPIB master, can be programmed to transfer images between video memory and the bus.

2. Hardware Description

The system includes nine MaxVideo modules and two Sarnoff-designed boards in a VME enclosure. This leaves nine additional slots free for future upgrades. Figure III-17 is a block diagram of the video processor.

The camera head provides 12-bit video data plus synchronizing signals to the video processor. The image processing modules process the incoming images with 16-bit accuracy and display an 8-bit part of the result.

The MaxVideo modules consist of: a video input module, five frame stores, a processing board, and a memory board and D/A set for display.

Maxscan 12 is a flexible analog and digital acquisition module. It can accept up to 16-bit digital data at up to 10-MHz clock rate. The input data and frame rate are completely programmable and will sync to the source signals. The module synchronizes the 9.75-MHz input data with the Maxbus clock.

Roistore 2048 is a programmable 16-bit frame store with dual-ported access for the host computer. Three modules are required in the system: one to store a frame of intercept corrections and one to store a frame of slope corrections, the third is used for dither and zoom operation.

Maxsp Mk II is a signal processing board with ALU, multiplier, lookup table, and barrel shifter. Output gain can be programmed using the barrel shifter. This module computes the 1- or 2-point correction compensation.

Modules can be added as future upgrades to provide other real-time processing capability. For example, a **FeatureMax** module provides for real-time histogram and feature list extraction, a **VFIR Mk II** convolution board can add 2-D filtering and/or pixel defect correction.

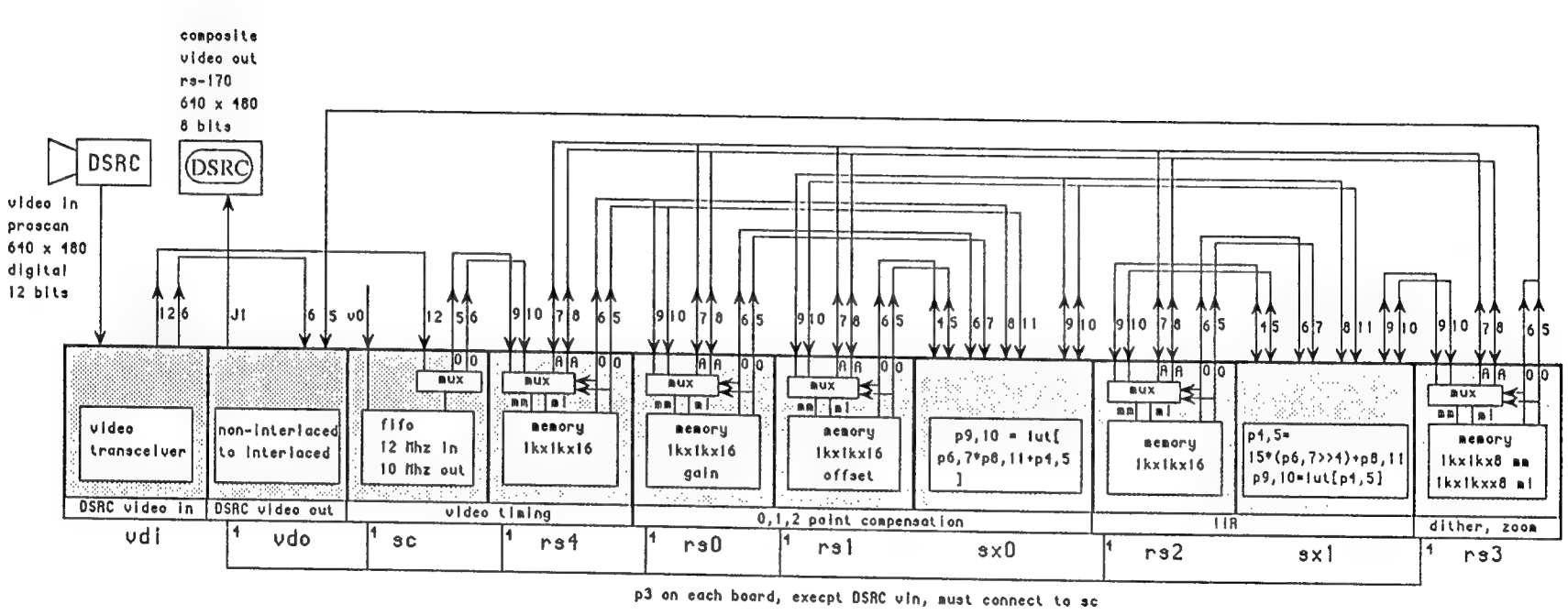


Figure III-17. *Block diagram of the video processor.*

3. Software

The software developed by Sarnoff for the IR camera system includes the following real time functions:

Initialization: A routine to set the processor in a default mode to display live video. Video may be displayed as raw input from the sensor, or processed according to some algorithm.

Buffer display: Contents of any frame buffer may be selected for display.

Store and load single-frame images to and from the host computer for non-real-time computation or for mass storage.

Frame averaging of successive frames to reduce noise. There are several options for computing the summation of 256 consecutive images. Since the input data is 12 bits and the data paths are16 bits, 16 consecutive summations of 16 images each are computed.

True sliding frame average of 2, 4, 8, or 16 frames is provided. Since the signal processing module allows several consecutive 16-bit operations such as (A x B + C), computing a frame average, adding the newest image and subtracting the oldest image, can be performed in a single pass through one module.

Compensation: Single point as well as provision for 12-bit slope and intercept correction compensation is incorporated. Single point correction compensation coefficients are computed internally. The coefficients for the slope and intercept method are computed on an external computer and transferred back to the processor/control box through the GPIB port.

Two-point compensation is performed as a single pass through one module, since the signal processor allows several consecutive 16-bit operations such as (A x B + C). The multiplier is software-programmable and takes two 16-bit operands to produce a full 32-bit result. This result is presented to a 32-bit barrel shifter that can window any 16 bits of the multiplier result. Provisions are available to output the entire 32-bit multiplier result.

Gain Control: The gain range is 1000:1 (60 dB). In the highest gain setting, 1200 electrons correspond to the full scale RS-170 output range, and in the lowest gain setting 1.2×10^6 electrons correspond to full output range. Steps of 2 dB are provided.

Display: The output module provides normal or inverted display of direct, compensated and compressed images. Freeze frame capability is also available. The output for display is available in analog RS-170 format based on an 8-bit window from the 16-bit data, or in 16-bit digital format. Black-and-white monitors with over- and under-scan capability are included.

Real-time dither and zoom: The video processor provides expanded display of the central quarter of image over the full display area so as to allow a one-half pixel x-dither, y-dither, xy-dither. The video memory has the ability to interleave pixels from two separate memory planes. Thus, by storing two images, one in the most significant byte and one in the least significant byte,

both images may be interleaved as a single output. Note that for the analog RS-170 only, the scan-converted output is restricted to 8 bits. The non-scan-converted 1- or 2-point compensated data retains full 12-bit accuracy.

GPIB port (IEEE 488): Uncompensated or compensated digital image data is available on the GPIB bus and through the direct digital read out. Offset memory (256 frame average) is available to the GPIB bus at 16-bit level. In addition, access to all other frame buffers and registers is available through the GPIB port.

Individual pixels are accessible through the GPIB port during the 1.2-ms RS-170 vertical blanking interval. Each pixel is read in < 100 μs, so that 10 pixels can be read from each field (20/frame).

Direct Digital Output: The differential 12-bit digital data with synchronization data from the camera head is buffered and output to the user per RS-422 differential data standard.

4. Power Consumption

The video processor/controller consumes < 500 W.

Section IV
SYSTEM MEASUREMENTS

A. NOISE EQUIVALENT TEMPERATURE DIFFERENCE

The camera rms video noise was measured at the processor output using a Rohde & Schwarz Video Noise Meter UPSF. This instrument measures the noise in a window that includes the center 55% of the 640 x 480 active pixels. This instrument was calibrated using a Hewlett Packard 437B Power Meter and a General Radio 1383 Random-Noise Generator with a carefully controlled noise band. The temperature difference measurement was made with the target at 27°C and 32°C using a Tektronix 1480 Waveform Monitor calibrated with the same power meter.

The Stirling No. 2 Camera had an NEΔT = 0.13° rms with the 3- to 5-µm filter installed. The change in photo current for the 5° temperature difference was 33 nanoamperes. Therefore the noise in electrons is 582 electrons rms per pixel.

The Multiband No. 2 Camera had an NEΔT = 0.26° rms with filter 8 (3 to 5 µm) selected. The photo current was not measured.

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